Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

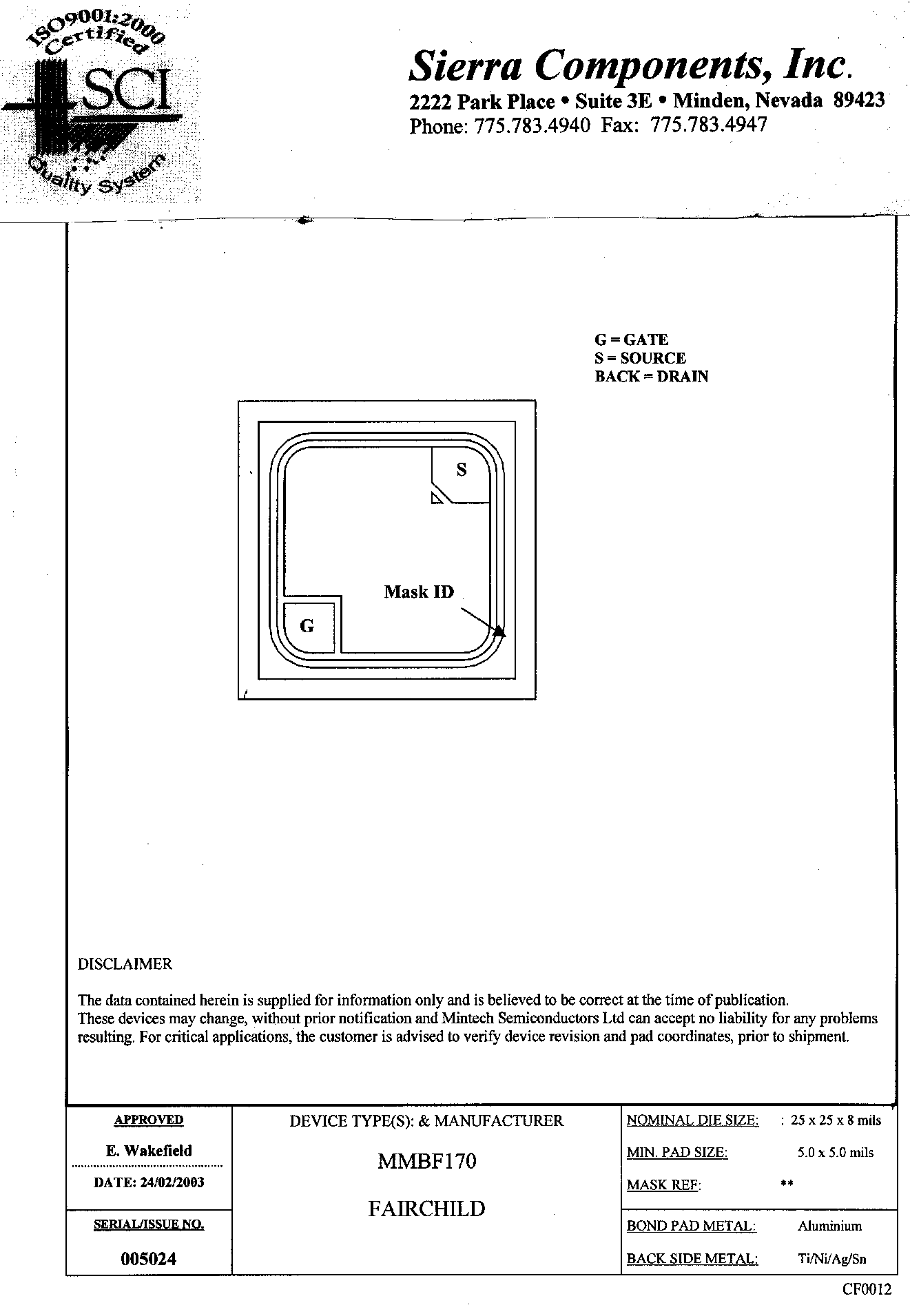
**PAD FUNCTIONS:**

**G = GATE**

**S = SOURCE**

**BACK = DRAIN**

**.025”**

****

**.025”**

**Top Material: Al**

**Backside Material: TiNiAgSn**

**Bond Pad Size: .005 X .005”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .025” X .025” DATE: 11/4/21**

**MFG: FAIRCHILD THICKNESS .008” P/N: MMBF170**

**DG 10.1.2**

#### Rev B, 7/1